

PROTECTION PRODUCTS

Description

The SMDA series of transient voltage suppressors are designed to protect components which are connected to data and transmission lines from voltage surges caused by ESD (electrostatic discharge), EFT (electrical fast transients), and lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The SMDA05-6 is designed to provide transient suppression on multiple data lines and I/O ports. It is designed to operate on 5V digital lines. The low profile SO-8 design allows the user to protect up to six data and I/O lines with one package.

The SMDA05-6 TVS diode array will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

Features

- ◆ 300 watts peak pulse power ($t_p = 8/20\mu s$)
- ◆ Transient protection for data lines to
IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 12A (8/20 μs)
- ◆ Protects up to 6 unidirectional lines
- ◆ Low operating voltage
- ◆ Low clamping voltage
- ◆ Solid-state silicon avalanche technology

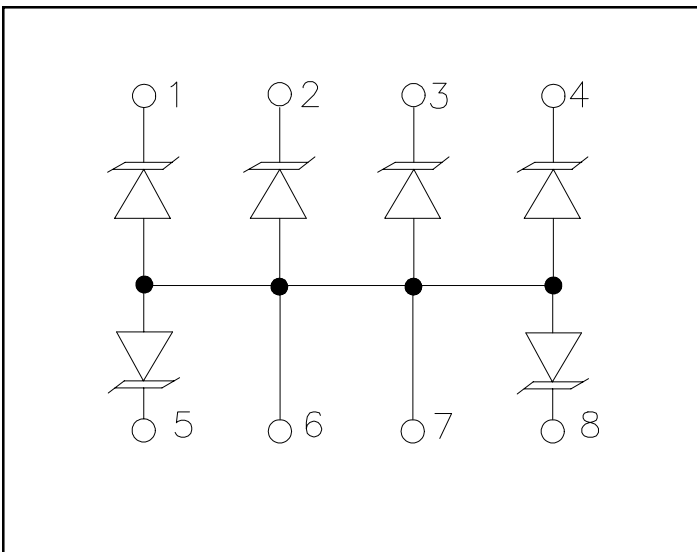
Mechanical Characteristics

- ◆ JEDEC SO-8 package
- ◆ UL 497B listed
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part number, date code, logo
- ◆ Packaging : Tube or Tape and Reel per EIA 481

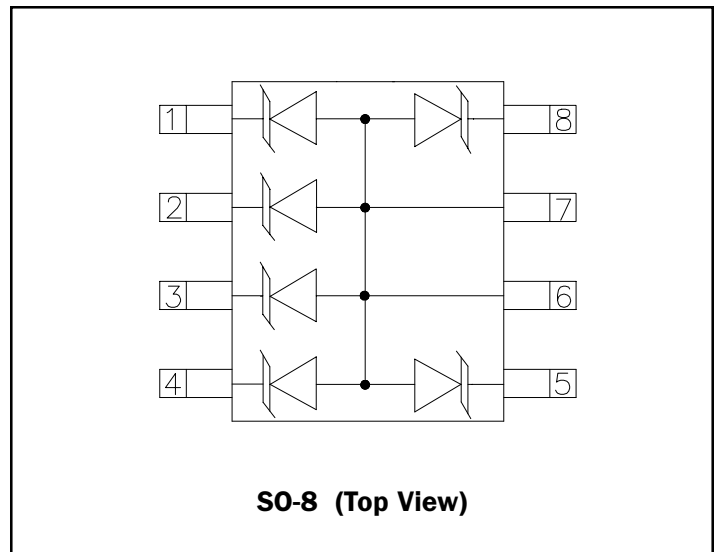
Applications

- ◆ 5V data & I/O lines
- ◆ Communication lines
- ◆ Microprocessor based equipment
- ◆ LAN/WAN equipment
- ◆ Servers
- ◆ Notebook & Desktop PC
- ◆ Instrumentation
- ◆ Peripherals

Circuit Diagram



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20μs)	I_{pp}	17	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

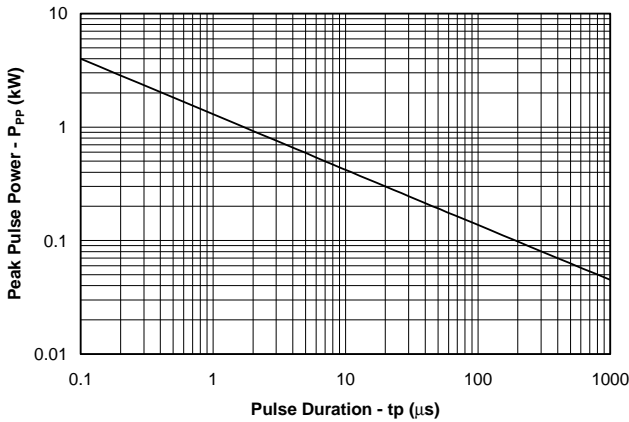
Electrical Characteristics

SMDA05-6						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^{\circ}C$			20	μA
Clamping Voltage	V_C	$I_{pp} = 1A, tp = 8/20\mu s$			9.8	V
Clamping Voltage	V_C	$I_{pp} = 5A, tp = 8/20\mu s$			11	V
Maximum Peak Pulse Current	I_{pp}	tp = 8/20μs			17	A
Junction Capacitance	C_J	Between I/O pins and Gnd $V_R = 0V, f = 1MHz$			400	pF

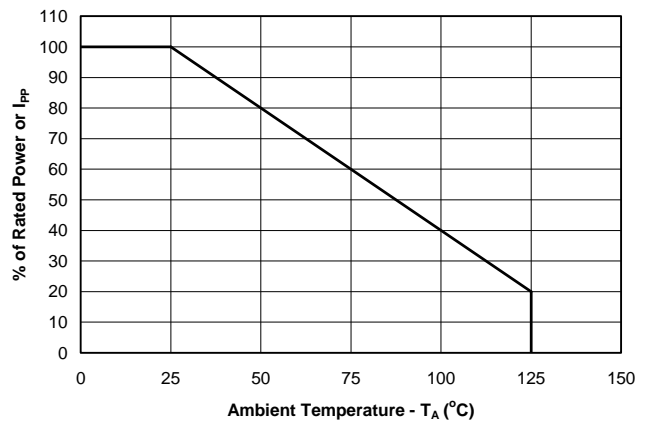
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Typical Characteristics

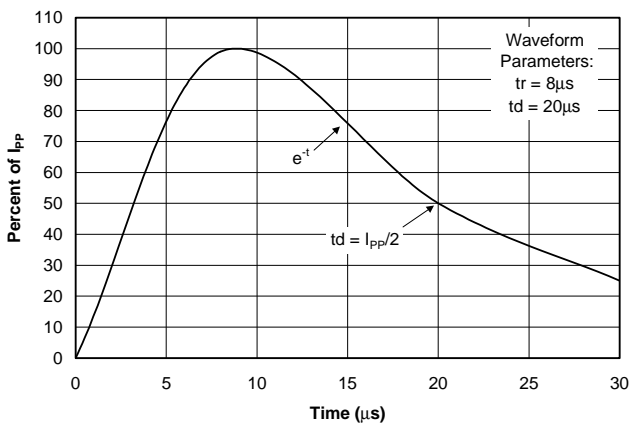
Non-Repetitive Peak Pulse Power vs. Pulse Time



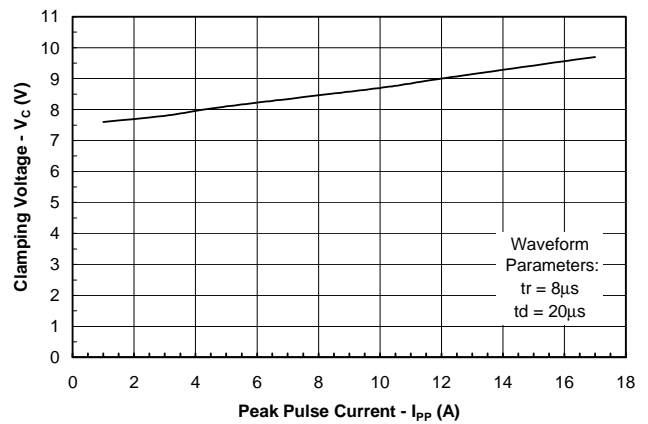
Power Derating Curve



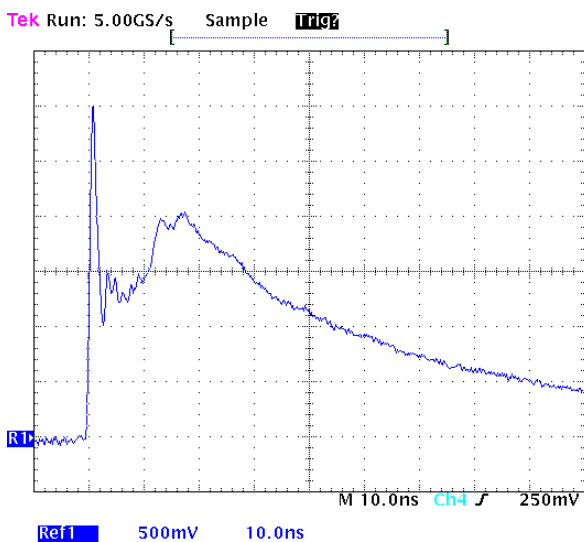
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



ESD Pulse Waveform (IEC 61000-4-2)



IEC 61000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

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Applications Information

Device Connection for Protection of Six Data Lines

The SMDA05-6 is designed to protect up to 6 data or I/O lines operating at 5 volts. They are unidirectional devices and may be used on lines where the signal polarities are above ground (i.e. 0 to 5V).

The device is connected as follows:

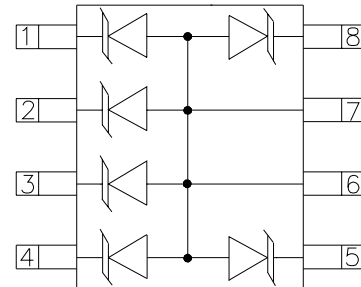
- Pins 1, 2, 3, 4, 5 and 8 are connected to the lines that are to be protected. Pins 6 and 7 are connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Board Layout Recommendations for Suppression of ESD.

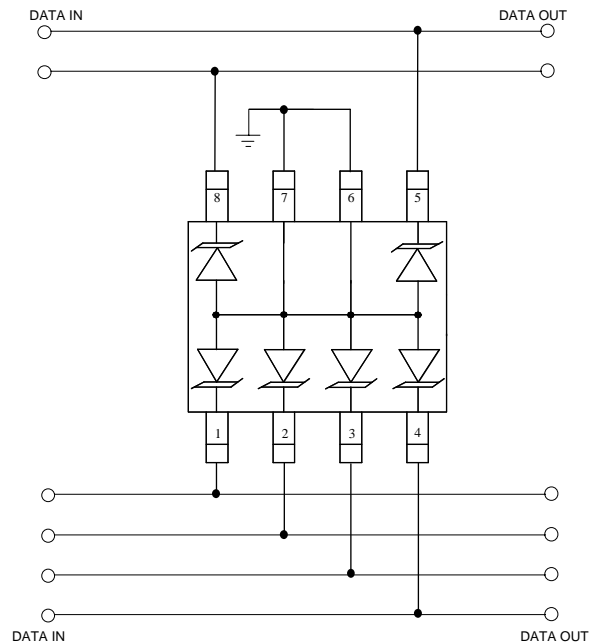
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Circuit Diagram

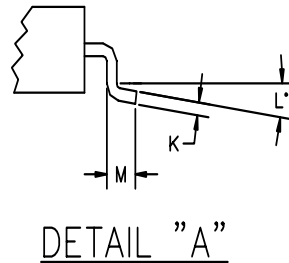
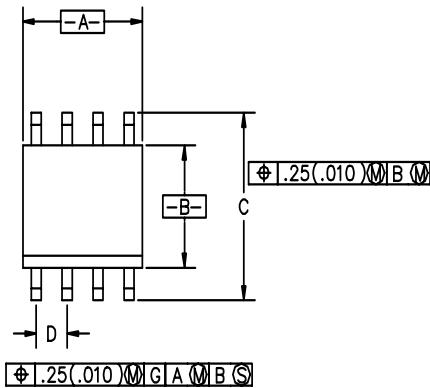


Connection Diagram

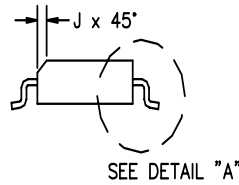
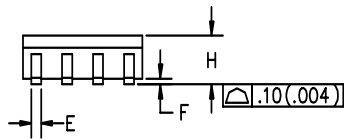


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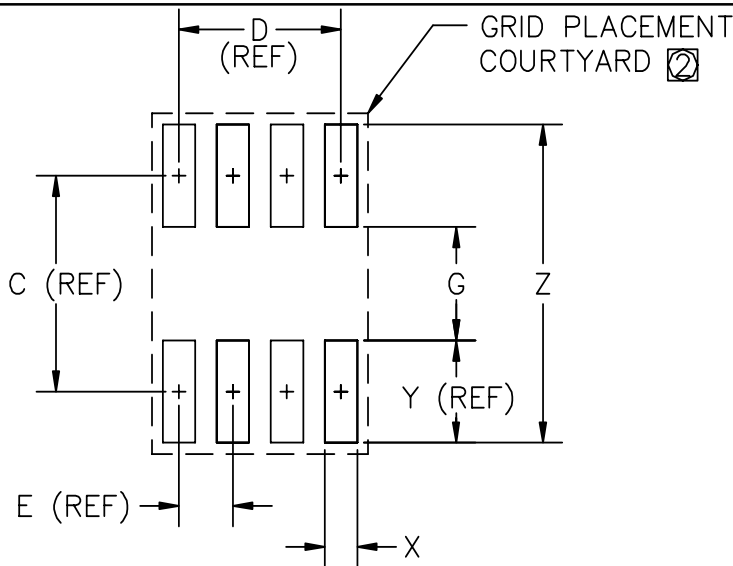
Outline Drawing - S0-8



DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	



Land Pattern - S0-8



DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.19	—	5.00	—
D	—	.15	—	3.81	—
E	—	.05	—	1.27	—
G	.10	.11	2.60	2.80	—
X	.02	.03	.60	.80	—
Y	—	.09	—	2.40	—
Z	—	.29	7.20	7.40	—

② GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

① CONTROLLING DIMENSION: MILLIMETERS

PROTECTION PRODUCTS**Ordering Information**

Part Number	Working Voltage	Qty per Reel	Reel Size
SMDA05-6.TB	5V	500	7 Inch
SMDA05-6.TE	5V	2,500	13 Inch

Note:

(1) No suffix indicates tube pack.

Contact Information

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